# CLAIMS

1. (Amended) A memory device characterized by comprising:

a non-volatile memory (11) including a plurality of memory blocks for storing data to which physical addresses are allocated, each of said blocks including physical pages, each of said physical pages including a logical page and a redundancy portion;

a translation table memory (123) which stores an address translation table (BPT) showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages;

a pointer memory (123) which specifies an empty page in a data storable state from among said pages and stores a write pointer (BSI) indicating a physical address of said specified empty page; and

a controller (12, S311, S314) which, when this memory system is activated, performs initializing process in which reads data from the redundancy portions of said non-volatile memory and prepares the address translation table in said translation table memory and the write pointer in said pointer memory, when to-be-written data and a logical address are supplied to said memory device, writes said to-be-written data in the empty page indicated by said write pointer, and renews said address translation table in such a way as to show a correlation between the physical address of that empty page and said logical address.

2. The memory device according to claim 1, characterized in that said controller (12) designates memory blocks from which data is to be erased from among those memory blocks which have data stored therein (S501), and discriminates whether data stored in said designated memory blocks is

valid or not, for each of those pages which constitute said designated memory blocks, transfers that data which has been discriminated as valid to another memory blocks (S502, S506), and erases that data which is stored in said designated memory blocks (S503).

3. The memory device according to claim 2, characterized in that said controller (12) discriminates whether or not the number of those memory blocks which do not have data stored therein becomes a number which does not satisfy a predetermined condition (S317), and

designates memory blocks from which data is to be erased from among data-storing

memory blocks when having discriminated that the number of said memory blocks which do not have data stored therein has become the number which does not satisfy said predetermined condition (S501).

4. The memory device according to claim 3, characterized in that said controller (12) writes an invalid flag indicating that data stored in a page to which a logical address has been allocated at a time to-be-written data and said logical address are supplied to said memory device is invalid in that page once (S310), and

said controller (12) designates an oldest-data storing memory block among those data-storing memory blocks which include pages where said invalid flag is written once, as a memory block from which data is to be erased (S501).

5. The memory device according to claim 4, characterized in that said controller (S502, S506) eliminates data stored in that page where said invalid flag is written once from those targets which are to be transferred to said another memory block.

6. The memory device according to claim 3, characterized in that a physical address includes block addresses indicating that block to which a page indicated by said physical address belongs, and block address are cyclically ordered, and

said controller (S501) designates, as a memory block from which data is to be erased, that one of data-storing memory blocks which is or follows a last block where data has been erased and to which a top block address is given.

7. The memory device according to claim 6, characterized in that said controller (12) writes an invalid flag indicating that data stored in a page to which a logical address has been allocated at a time to-be-written data and said logical address are supplied to said memory device is invalid in that page once (S310), and

eliminates data stored in that page where said invalid flag is written once from those targets which are to be transferred to said another memory block (S502, S506).

8. The memory device according to claim 6, characterized in that said controller (12) writes a logical address supplied to said memory device in that page where said to-be-

written data has been written (S314), and

discriminates whether or not said logical address stored in said page coincides with that logical address which is associated with the physical address of that page in said address translation table, and eliminates data stored in that page from those targets which are to be transferred to said another memory block when having discriminated that there is no coincidence (S501, S502, S506).

9. The memory device according to claim 8, characterized in that physical addresses are cyclically ordered, and

said pointer memory (123) specifies a top one of those empty pages which are given physical addresses equal to or following the physical address of that page where data is written.

10. The memory device according to claim 9, characterized in that when the logical address of a to-be-read page is supplied to said memory device, a physical address associated with said logical address is specified based on said address translation table and data is read out from that page which is indicated by said specified physical address and is sent outside (S206 to S214).

11. The memory device according to claim 9, characterized in that when the logical address of a to-be-read page is supplied to said memory device, that page which is given said logical address is specified based on said address translation table and data is read out from said specified page and is sent outside (S206 to S214).

12. The memory device according to claim 11, characterized in that said address translation table shows a correlation between predetermined upper digits of the physical address of each page and the logical address of that page,

said controller (12) writes a logical address supplied to said memory device in that page where said to-be-written data has been written; and

when the logical address of a to-be-read page is supplied to said memory device, a value of said predetermined upper digits of the physical address associated with said logical

address is specified based on said address translation table and data is read out from that page which is included in individual pages each having a physical address whose upper digits coincide with said specified value and in which said logical address of said to-be-read page is written, and is sent outside (S206 to S214).

13. The memory device according to claim 12, characterized in that said controller (12) writes an invalid flag indicating that data stored in a page to which a logical address has been allocated at a time to-be-written data and said logical address are supplied to said memory device is invalid in that page once (S310), and

data is read out from that page which is included in individual pages each having a physical address whose upper digits coincide with said specified value and in which said logical address of said to-be-read page is written and said invalid flag is not written, and is sent outside (S206 to S214).

14. The memory device according to claim 8, characterized in that physical addresses are cyclically ordered,

said pointer memory (123) specifies a top one of those empty pages which are given physical addresses equal to or following the physical address of that page where data is written, and

said controller (12) reads out data from a lowest-ordered page in those individual pages each having a physical address whose upper digits coincide with said specified value and in which said logical address of said to-be-read page is written, and sends said data outside (S206 to S214).

15. The memory device according to claim 11, characterized in that said address translation table shows a correlation between predetermined lower digits of the physical address of each page and the logical address of that page, and a range over which a value of a physical address can be associated with a logical address is determined for each logical address, and

when the logical address of a to-be-read page is supplied to said memory device,

said controller (S206 to S214) specifies a value of said predetermined lower digits of the physical address associated with said logical address is specified based on said address translation table, and reads out data from that page which is included in individual pages each having a physical address whose lower digits coincide with said specified value and which is given a physical address lying in said range, and sends that data outside.

16. The memory device according to claim 15, characterized in that said translation table memory (123) is constituted by a non-volatile memory which stores said address translation table.

17. The memory device according to claim 15, characterized in that said translation table memory (123) is constituted by the page that stores said address translation table, and

said controller (S310 to S312) reads at least a part of said address translation table from said page, renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address and writes said renewed part in another empty page (S601 to S603).

18. The memory device according to claim 17, characterized in that said controller (12) stores an address translation table storage location list showing physical addresses of those pages which store data constituting said address translation table (S105B),

reads at least a part of said address translation table from that page which is given a physical address indicated by said address translation table storage location list, renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address and writes said renewed part in another empty page, and

renews said address translation table storage location list in such a way as to show the physical address of said another empty page (S602, S603).

19. The memory device according to claim 17, characterized in that a range of a value of upper digits of the physical address of each of those pages which store data constituting said address translation table is predetermined,

said controller (12) stores an address translation table storage location list showing predetermined lower digits of the physical address of each of those pages which store data constituting said address translation table (S105B),

reads at least a part of said address translation table from that page which is included in pages each having a physical address whose predetermined lower digits are specified by said address translation table storage location list and the predetermined upper digits of the physical address of which lies in said range, renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address and writes said renewed part in another empty page, and

renews said address translation table storage location list in such a way as to show the physical address of said another empty page (S602, S603).

20. The memory device according to claim 19, characterized in that said controller (S601 to S603) specifies that page which stores a part showing a correlation between said logical address supplied to said memory device and said physical address from among those pages which have said address translation table stored therein, reads only that part which is stored in said specified page, renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address and writes said renewed part in another empty page.

21. The memory device according to claim 20, characterized by further comprising a non-volatile memory (123) which stores an empty block table containing information for identifying that memory block which does not have data stored therein, and

in that said controller (12), further, discriminates whether or not writing to-be-written data supplied to said memory device in an empty page has resulted in that the memory block which includes said empty page has no further empty page, and renews said empty block table in such a way as to indicate that said memory block including said empty block has said data stored therein, when having discriminated that said memory block

including said empty block has no further empty page (S315, S316), and

renews said empty block table in such a way as to indicate that a memory block from which data to be stored has been erased does not have that data stored therein.

22. The memory device according to claim 20, characterized in that some of said pages constitute empty block table memory means (11) which stores an empty block table containing information for identifying that memory block which does not have data stored therein, and

said controller (12), further, discriminates whether or not writing to-be-written data supplied to said memory device in an empty page has resulted in that the memory block which includes said empty page has no further empty page, and, when having discriminated that there is no further empty page, reads at least a part of said empty block table from said empty block table means, renews said empty block table in such a way as to indicate that said memory block including said empty block has said data stored therein, and stores said renewed empty block table in said empty block table means (S315, S316), and

reads at least a part of said empty block table from said empty block table means, renews said empty block table in such a way as to indicate that a memory block from which data to be stored has been erased does not have said data stored therein, and stores said renewed empty block table in said empty block table means (S504).

23. The memory device according to claim 22, characterized in that said controller (12) stores an empty block table pointer indicating the physical address of a page storing that data which constitutes said empty block table (S107), and reads at least a part of said empty block table from that page which is given said physical address indicated by said empty block table pointer.

24. The memory device according to claim 22, characterized in that a range of a value of upper digits of the physical address of each of those pages which store data constituting said address translation table is predetermined, and

said controller (12) stores an empty block table pointer indicating predetermined

lower digits of the physical address of a page storing that data which constitutes said empty block table (S107), and reads at least a part of said empty block table from that page which is included in pages each having a physical address whose lower digits are specified by said empty block table pointer and which has a physical address whose upper digits lie in said range (S308).

25. The memory device according to claim 24, characterized in that said controller (12) specifies that page in which a to-be-renewed part in said stored empty block table is stored from among those pages which have said empty block table stored therein, and reads out only that part which is stored in said specified page.

26. (Amended) A memory managing method for managing a non-volatile memory having a plurality of memory blocks for storing data to which physical addresses are allocated, and each of said memory blocks including physical pages, each of said physical pages including a logical page and a redundancy portion, characterized in that

said method comprises the steps of:

when said non-volatile memory is activated, reading data from the redundancy portions of said non-volatile memory and preparing an address translation table showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages and a write pointer indicating a physical address of an empty page,

receiving to-be-written data and logical address; and

when to-be-written data and a logical address are supplied, writing said to-be-written data in the empty page indicated by said write pointer, and said address translation table is renewed in such a way as to show a correlation between the physical address of that empty page and said logical address

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(S311, S314).

27. (Amended) The memory managing method according to claim 26, characterized in that memory blocks from which data is to be erased is designated from among those memory blocks which have data stored therein (S501), and

discriminating whether data stored in said designated memory blocks is valid or not, for each of those pages which constitute said designated memory blocks, transferring that data which has been discriminated as valid to another memory blocks, and erasing that

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data which is stored in said designated memory blocks (S502, S506, S503).

28. (Amended) The memory managing method according to claim 27, characterized in that discriminating whether or not the number of those memory blocks which do not have data stored therein becomes a number which does not satisfy a predetermined condition (S317), and

when it is discriminated that the number of said memory blocks which do not have data stored therein has become the number which does not satisfy said predetermined condition, designating a memory block from which data is to be erased from among data-storing memory blocks (S501).

29. A program for allowing a computer (121), connected to a memory (11) including a plurality of memory blocks for storing data to which physical addresses are allocated, to function to:

store an address translation table showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages (S105);

specify an empty page in a data storable state from among said pages and store a write pointer indicating a physical address of said specified empty page (S107); and

when to-be-written data and a logical address are supplied to said computer, write said to-be-written data in the empty page indicated by said write pointer and renew said address translation table in such a way as to show a correlation between the physical address of that empty page and said logical address (S311, S314).

30. The program according to claim 29, characterized in that said program designates memory blocks from which data is to be erased from among those memory blocks which have data stored therein (S501), and

discriminates whether data stored in said designated memory blocks is

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valid or not, for each of those pages which constitute said designated memory blocks, transfers that data which has been discriminated as valid to another memory blocks, and erases that data

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which is stored in said designated memory blocks (S502, S506, S503).

31. The program according to claim 30, characterized in that said program discriminates whether or not the number of those memory blocks which do not have data stored therein becomes a number which does not satisfy a predetermined condition (S317), and

designates memory blocks from which data is to be erased from among data-storing memory blocks when having discriminated that the number of said memory blocks which do not have data stored therein has become the number which does not satisfy said predetermined condition (S501).